REMARKS/ARGUMENTS

This Amendment is being filed in response to the Decision from the Board of Patent Appeals and Interferences of January 11, 2010. Reconsideration and allowance of the application in view of the amendments made above and the remarks to follow are respectfully requested.

Claims 1 and 3-5 are pending in the Application. Claims 1 and 4 are independent claims. Claim 2 is canceled herein, without prejudice. The Applicants respectfully reserve the right to reintroduce subject matter deleted herein, either at a later time during the prosecution of this application or any continuing applications.

By means of the present amendment, the claims are amended to clarify the recitations contained therein.

Claims 1 - 5 are rejected under 35 U.S.C. §102(b) over U.S. Patent No. 4,876,643 to McNeill et al. ("McNeill") and over U.S. Patent No. 6,266,766 to O'Connor ("O'Connor"). These rejections are respectfully traversed. It is respectfully submitted that claims 1 and 3-5 are allowable over McNeill and over O'Connor for at least the following reasons.

In rejecting the claims in view of McNeill, the Office Action dated September 30, 2005 (hereinafter, "the Office Action") cites McNeill, col. 7 lines 5-20. It is respectfully submitted that reliance on this portion of NcNeill or any section for that matter is misplaced.

McNeill, col. 7 lines 5-20, states:

> When the slave processor 212 receives a search record assignment from the master processor 210 it enters the SETUP SEARCH STATE TABLES state 252. In the state 252, the slave processor 212 takes the search pattern from the master processor 210 and initializes its internal state in preparation for search processing. Once the slave processor 212 has completed its initialization, it

> enters the WAIT FOR NEXT RECORD IN DATA LIST STREAM 254 state. In the state 254, the slave processor 212 performs initializations which must take place immediately before each record to be processed and then waits for the signal from the master processor 210 indicating the start of the next record. This signal sends the slave processor 212 into the PROCESSOR RECORD state 256. A detailed expansion of this state 256 is shown in FIG. 7.

While the referenced section discusses searches performed by slave processors, it is respectfully submitted that this section fails, as the rest of McNeill to disclose that which is recited in the claims.

In rejecting claim 2 of the present application, the Office Action cites O'Connor, col. 1, lines 54-61 which states:

> Bypassing is used where a processor contains some collection of data in a register file and also contains a set of execution units, each of which may take a varying amount of time to complete an operation. An execution unit can take a varying amount of time to complete an operation because, for example, the execution unit is a multicycle execution unit or because the processor has a pipelined implementation where no operation finishes immediately.

So while the cited section of O'Connor describes an execution unit that may take varying amounts of time, this has little or nothing to do with that which is recited in claim 1.

It is respectfully submitted that the apparatus of claim 1 is not anticipated or made obvious by the teachings of McNeill and O'Connor. For example, McNeill and O'Connor do not disclose or suggest, an apparatus that amongst other patentable elements, comprises (illustrative emphasis added)

> a first functional unit for performing one or more operations having a relatively large latency, the first functional unit including a slave controller;
>
> a second functional unit for performing one or more operations having a relatively small latency;
>
> a common memory means shared by the first and second functional units; and

> a master controller for controlling a schedule for executing an instruction by the first functional unit, the execution of said instruction including input/output operations that are performed by the slave controller of the first functional unit,
>
> wherein said master controller synchronizes at least one of output data of the first functional unit processed by the second functional unit during the execution of said instruction and the input data to the first functional unit being generated by the second functional unit during the execution of said instruction.

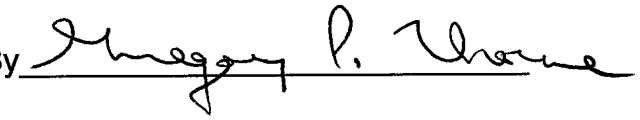
as recited in claim 1, and as similarly recited in claim 4.

Based on the foregoing, the Applicant respectfully submits that independent claims 1 and 4 are patentable and notice to this effect is earnestly solicited. Claims 3 and 5 respectively depend from one of claims 1 and 4 and accordingly are allowable for at least this reason as well as for the separately patentable elements contained in each of the claims. Accordingly, separate consideration of each of the dependent claims is respectfully requested.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

Applicants have made a diligent and sincere effort to place this application in condition for immediate allowance and notice to this effect is earnestly solicited.

Respectfully submitted,

By 

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March 8, 2010

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